High Gain Operational Amplifier Using Enhancement and Depletion Mode a-IGZO TFTs

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Abstract

***An operational amplifier (OpAmp) consisting of twenty-two dual gate amorphous IGZO (a-IGZO) thin-film transistors (TFTs) is fabricated on a glass substrate. To achieve high voltage gains enhancement and depletion mode transistors are used. The enhancement mode TFTs work as drivers and the depletion mode TFTs act as depletion loads in the OpAmp circuit. The created OpAmp has a voltage gain (G) of 54.80 dB, a cutoff frequency (f_c) of 75 Hz, a unity gain frequency (f_{ug}) of 10 kHz and a slew rate t_s(up/down) of 0.15/0.30 V/µs. Transistors with different threshold voltages U_{th} on the same substrates are realized by using different semiconductor channel thicknesses. This is possible, as an increasing layer thickness of the semiconductor leads to a reduction of the threshold voltage U_{th}* [1].**

Author Keywords

Operational amplifier; Dual gate amorphous IGZO thin-film transistors; Thin-film circuits; Inverter; Enhancement load; Depletion load

1. Introduction

High-gain and high-frequency amplifiers will be a key building block for applications like active-matrix liquid crystal displays or sensor arrays. Using a-IGZO as semiconductor material has many advantages such as high device performance because of its high field-effect mobility, low leakage current, production at low temperatures and optical transparency **[2]**. Another import point are low production costs. Because of these advantages a-IGZO TFTs and related circuits have the potential to take a major role in digital and analog electronic industry.

To realize high performance circuits typically CMOS-technology is used. This is not possible because a-IGZO has a negligible hole mobility **[2]**. In order to realize high-performance circuits, depletion- and enhancement-mode nMOS transistors are required instead. One way to adjust the threshold voltage of a-IGZO TFT is to vary the thickness of the semiconductor film **[1]**. With increasing film thickness the threshold voltage U_{th} decreases (**Fig 1.**).

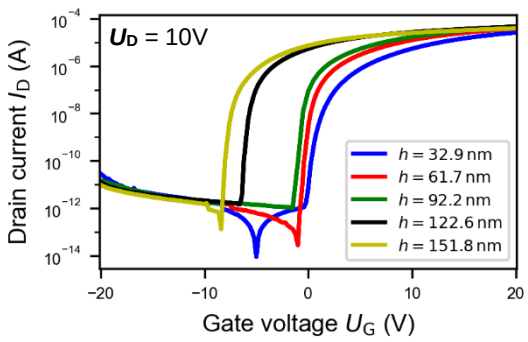

Figure 1. Input characteristics $I_D(U_G)$ of dual gate TFTs with a channel width w = 10 µm, a channel length l = 10 µm and varying channel thickness h.

At first the fabrication of the used transistors is discussed in this paper. Then the electronical properties like input and output characteristics are analyzed. Next, inverter circuits are demonstrated to show the advantages of using depletion loads instead of enhancement loads **[3]**. Afterwards the design of the OpAmp circuit is discussed. The main part of this paper is dealing with the performance analysis of the created OpAmp. Therefore, the figures of merit like the open loop gain G, cutoff frequency f_c, unity gain frequency f_{ug}, phase margin PM, gain-bandwidth product $GBWP$ and the slew rate t_s**(up/down)** are given.

2. TFT fabrication

The layer structure (cross-sectional view) of the enhancement and the depletion type TFTs investigated in this work is shown in **Fig. 2 (a)** and **(b)** respectively. It can be seen that the only difference is the thickness of the semiconductor layer. To realize two different layer thicknesses of the same material an additional photolithography step is needed.

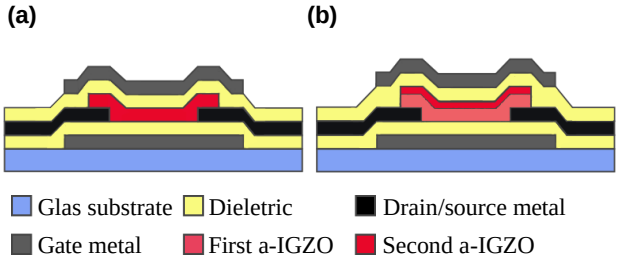

Figure 2. Cross section view: **(a)** Enhancement mode dual gate a-IGZO TFT with channel thickness h of 33 nm. **(b)** Depletion mode dual gate a-IGZO TFT with a channel thickness h of 162 nm.

At first a 70 nm thick MoTa layer is deposited using RF magnetron sputtering. Afterwards the layer is structured to form the bottom gate. Next a double layer consisting of 175 nm SiN and 50 nm SiOx is placed as a bottom dielectric. This layer is created by plasma enhanced chemical vapor deposition (PECVD) at 280 °C.

Then the drain and source are manufactured as a double layer of 70 nm MoTa and 50 nm ITO. The fabrication process is adjusted in such a way that only ITO is in contact with the later deposited a-IGZO channel. Before the IGZO layer is added to the layer structure the substrates are tempered for one hour at 250 °C. This tempering step has the purpose to increase the conductivity of the ITO layer. A good ohmic contact to the semiconductor should be created.

A-IGZO is deposited using RF magnetron sputtering from a solid state (1:1:1 mol %)-IGZO target. In contrast to the depletion mode TFTs for the enhancement TFTs the first IGZO layer is etched completely away. Then a second layer of IGZO is added and structured. By this process single and double layered transistors are created. After the creation of the semiconductor channel the substrates are annealed for two

hours at 300 °C. To isolate the top gate a layer of 130 nm SiOx is used. This layer is placed via PECVD at 250 °C. The temperature is decreased in comparison to the deposition of the bottom dielectric to minimize negative influences on the semiconductor. As top gate a double layer of 70 nm MoTa and 50 nm ITO is employed. As a last step the transistors are baked overnight (around sixteen to eighteen hours) at 250 °C. During the tempering steps oxygen atoms diffuse into the IGZO layer and oxygen vacancies are occupied. Free electrons are bound and the conductivity is decreased. This yields to a slightly positive threshold voltage of the dual gate a-IGZO transistors with a channel thickness h of 36 nm.

3. TFT characteristics

In **Fig. 3** the input and output characteristics of the created transistors are shown. It can be seen that the enhancement mode transistors (w = 10 µm, l = 10 µm, h = 33 nm) have threshold voltages U_{th} in the range of 1.72 V to 2.43 V. The measured field-effect mobilities μ are ranging from 11.53 cm²/(Vs) to 12.65 cm²/(Vs). The five identically constructed enhancement type transistors show good homogeneity. In comparison the homogeneity of the five depletion mode TFTs (w = 10 µm, l = 100 µm, h = 162 nm) is slightly reduced. The determined threshold voltages U_{th} are ranging from -3.82 V to -3.47 V. The field effect mobilities μ are between 12.04 cm²/(Vs) and 14.20 cm²/(Vs).

The depletion type transistors are used as depletion loads in the OpAmp circuit. To work as a depletion load, the gate is connected to the source of the transistor. For this reason, the output curve $I_D(U_D)$ for a gate voltage of 0 V is of interest. In **Fig. 3 (b)** the output curve $I_D(U_D)$ for five identically constructed depletion type TFTs are illustrated. It can be seen that for drain voltages U_D > 4 V the drain current stays almost the same. In this drain voltage area, the depletion loads act approximately as ideal current sources.

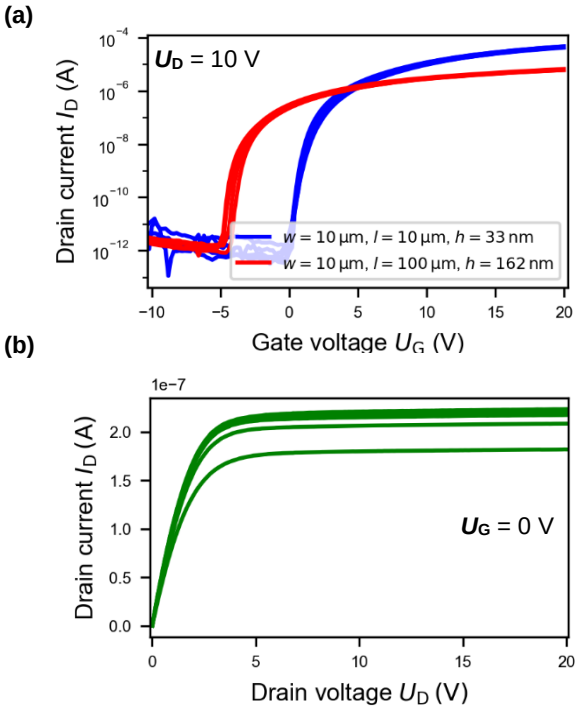

Figure 3. (a) Input characteristics $I_D(U_G)$ of respectively five identically constructed enhancement- and depletion- mode TFTs. **(b)** Output characteristics $I_D(U_D)$ of depletion type dual gate transistors with a channel width w of 10 µm, a channel length l of 100 µm and a channel thickness h of 162 nm. The gate voltage U_G is set to 0 V.

4. Inverter

An nMOS inverter is composed of a driver transistor (enhancement mode) and a load connected in series. This load can also be realized by a second transistor. The mode of this second load transistor (enhancement or depletion) has a major influence on the properties of the created inverter. If an enhancement load is implemented the gate of the load transistor is connected to U_{DD} **(Fig. 4 (a))**. In contrast if a depletion load is used the gate of the load transistor is connected to the output node U_{out} **(Fig. 4 (b)) [3]**.

In **Fig 4 (c)** the voltage transfer characteristic curves of one inverter with an enhancement and one with a depletion load are shown. All used transistors have a width w of 10 µm and a length l of 10 µm. The enhancement mode TFT have a thickness h of 44.3 nm. The thickness of the depletion mode TFT is 93.55 nm. A voltage equal to 10 V is applied to U_{DD}. The node U_{SS} is set to -10 V.

The depletion load inverter shows much wider swing range and larger voltage gain than the enhancement load inverter. The voltage gains G are 23.28 dB and 0.07 dB, while their output swing ranges are -9.96 V to 9.94 V and -4.49 V to 8.04 V respectively.

These results show that inverters with depletion load are superior to inverters with enhancement load **[4]**. This insight motivates the usage of depletion loads in the OpAmp circuit. To realize a high gain operational amplifier the combination of driver transistors (enhancement mode) and depletion loads is required or at least advantageous.

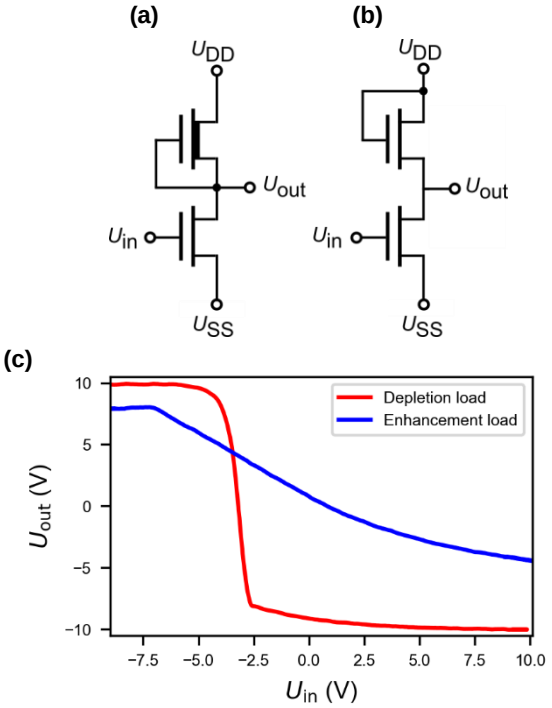

Figure 4. Circuit diagram: **(a)** Inverter with a depletion load. **(b)** Inverter with an enhancement load. **(c)** Voltage transfer curves one enhancement load inverter and of one depletion load inverter.

5. OpAmp design

In **Fig. 5** the circuit diagram of the OpAmp is shown. The presented OpAmp design consists of four different stages **[11]**. As input stage a differential amplifier with a negative feedback loop is implemented. The output voltage of the input stage is the amplified potential difference between the two inputs $U_{in,+}$ and $U_{in,-}$. The needed bias voltage to control the current source (T_5) of the input stage is created by an nMOS voltage divider connected to the supply voltage.

The second stage is a push-pull stage. This stage converts the differential signal from the input stage into a single signal. The push-pull stage is followed by the amplifier stage, which amplifies the input signal. As final stage an output stage is used. The output stage should be able to drive a large output current with a small output resistance.

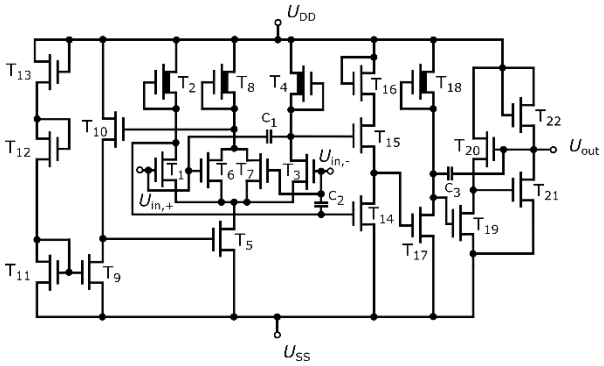

Figure 5. OpAmp circuit design **[11]**. The design consists of four stages: 1. Differential amplifier, 2. Push-pull stage, 3. Amplifier stage, 4. Output stage.

In total twenty-two TFTs and three capacities (C1, C2 and C3 equals 0.5 pF) are used. Four of the transistors are depletion mode transistors and the others are enhancement mode transistors with different geometries. As semiconductor layer thickness ***h*** a value of 33 nm for the enhancement mode TFTs and a value of 162 nm for the depletion mode TFTs is chosen. The gates of the depletion mode TFTs are connected to their sources so that they act like depletion loads.

In **Tab. 1** the geometry and the mode (E for enhancement and D for depletion) of all integrated TFTs are listed.

Table 1. Geometry of the TFTs used for the OpAmp.

***w/l* (µm)**	**TFT Nr.**
10/10 E	T_9, T_{10}, T_{11}, T_{13}, T_{14}, T_{15}, T_{17}
100/10 E	T_1, T_3, T_5, T_6, T_7
40/10 E	T_{19}
50/10 E	T_{12}
500/10 E	T_{21}
10/20 E	T_{16}
10/40 E	T_{20}, T_{22}
50/10 D	T_2, T_4, T_8, T_{18}

6. Results and discussion

The measured DC transfer characteristic ($\boldsymbol{U_{out}(U_{in,+} - U_{in,-})}$) of the OpAmp is shown in **Fig. 6 (a).** To bias the OpAmp 11.88 V is applied to $\boldsymbol{U_{DD}}$ and – 7.97 V to $\boldsymbol{U_{SS}}$. It can be seen that the swing range (-5.57 V to 8.97 V) of the OpAmp is smaller than the supply voltage. The measured voltage gain amounts 77.79 dB. The input referred offset is 44.53 mV. This value is the needed potential difference between the two inputs $\boldsymbol{U_{in,+}}$ and $\boldsymbol{U_{in,-}}$ to get an value of 0 V at the output. The reason for this is that due to production imperfections the TFTs T_1 and T_3 or T_2 and T_4 have different threshold voltages. The OpAmp is tested as a comparator (**Fig. 6 (b)**). A sinusoidal differential signal of 1 V_{pp} (peak to peak) is applied to the inputs. This signal is created by a common waveform generator. An oscilloscope is used to measure the output signal $\boldsymbol{U_{out}}$.

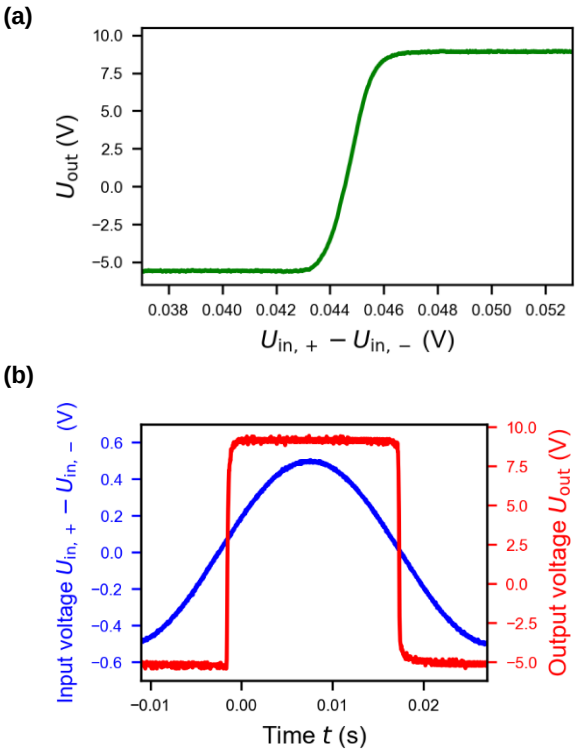

Figure 6. (a) DC transfer characteristic of the OpAmp. The measured open loop gain is 77.79 dB. The input referred offset is 44.53 mV. **(b)** OpAmp used as comparator. Output signal $\boldsymbol{U_{out}}$ measured for a sinusoidal differential input of 1 V_{pp} with a frequency ***f*** of 10 Hz.

In **Fig. 7 (a)** gain and phase response of the output stage dependent on the frequency ***f*** is shown. For low frequencies ***f*** the OpAmp has a gain of 54.80 dB. At the frequency $\boldsymbol{f_c}$ = 75 Hz, the gain ***G*** is decreased by -3 dB. From this frequency the gain ***G*** decreases with a slope of -20 dB per decade. This decrease is the expected behavior of a first order low pass filter. For frequencies higher than 8 kHz the gain decreases with a higher slope. As unity gain frequency $\boldsymbol{f_{ug}}$ a value of 10 kHz is determined. The gain-bandwidth product ***GBWP*** is 70 kHz. The phase difference ***P*** between input signal and output signal is really close to zero for frequencies smaller than the cutoff frequency $\boldsymbol{f_c}$. With increasing frequency ***f*** the absolute phase lag is increasing. At 6.5 kHz the output is shifted by -180°. The phase margin ***PM*** of the OpAmp amounts -48.24°.

In Fig **7. (b)** the frequency dependent gain for the three prior stages (input stage, push-pull stage and amplifier stage) are presented. This analysis is used to verify if all stages are working as expected. A major drawback might be an attenuation instead of an amplification of a certain stage. The differential amplifier stage yields an amplification by a factor of 276.14 (48.82 dB). The push-pull stage does not lead to an increase in the amplification. However, the signal is also not strongly decreased. The amplifier stage raises the gain ***G*** to over 50 dB. These results prove that all stages are addressed in their operating voltage ranges, as there is no significant decrease of gain ***G*** at either stage.

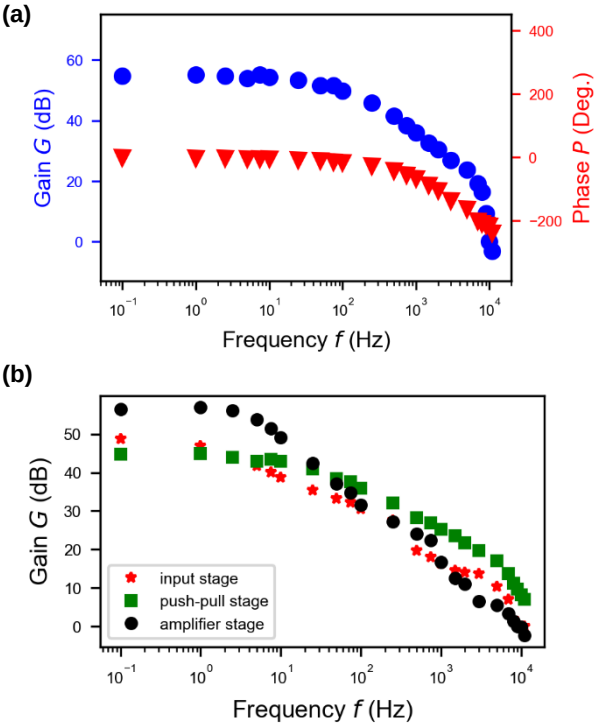

Figure 7. (a) Gain ***G*** and phase ***P*** response of the output stage dependent on the frequency ***f***. **(b)** Frequency dependent gain ***G(f)*** of the prior stages (input stage, push-pull stage, amplifier stage).

Another parameter of an OpAmp is the slew rate t_s. This parameter describes how fast the output of the operational amplifier can react to a voltage change at the inputs. To measure this value a rectangular signal (extremely low-rise time) is placed at the non-inverting input, while the inverting input is set to 0 V. The slew rate is equal to the extrema of the output signal slope. The determined slew rate t_s**(up/down)** is equal to 0.15/0.30 V/µs. If the derived figures of merit of the shown depletion load OpAmp are compared to results from other papers **[3-7]** and **[10]** it can be seen that the open loop gain ***G*** is much higher in comparison to all-enhancement TFT operational amplifier designs. As a trade off the cut off frequency f_c and the unity gain frequency f_{ug} are smaller. The slew rate t_s is in a comparable range to previous works.

7. Conclusion

This paper presented an OpAmp which uses depletion mode a-IGZO TFTs as loads and enhancement mode a-IGZO TFTs as drivers. The fabricated OpAmp has an open loop voltage gain ***G*** of 54.80 dB, a cutoff frequency f_c of 75 Hz, a unity gain frequency f_{ug} of 10 kHz and a slew rate t_s**(up/down)** of 0.15/0.3 V/µs. The much higher open loop gain in comparison to all enhancement OpAmp designs is the main benefit of using depletion loads. In this work the threshold voltage of the TFTs is controlled via the layer thickness of the semiconductor. The drawback of this technique is that an additional lithography step is required to create enhancement and depletion mode transistors on the same substrate.

8. Acknowledgement

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9. References

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