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Growth of telecom C-band In(Ga)As quantum dots for silicon quantum photonics

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Abstract

Photonic integrated circuits (PICs) based on the silicon-on-insulator platform currently allow high-density integration of optical and electro-optical components on the same chip. This high complexity is also transferred to quantum PICs, where non-linear processes are used for the generation of quantum light on the silicon chip. However, these intrinsically probabilistic light emission processes pose challenges to the ultimately achievable scalability. Here, an interesting solution would be employing on-demand sources of quantum light based on III–V platforms, which are nonetheless very complex to grow directly on silicon. In this paper, we show the integration of InAs quantum dots (QDs) on silicon via the growth on a wafer-bonded GaAs/Si template. To ensure emission in the telecom C-band (∼1550 nm), a metamorphic buffer layer approach is utilized. We show that the deposited single QDs show similar performance to their counterparts directly grown on the well-established GaAs platform. Our results demonstrate that on-demand telecom emitters can be directly and effectively integrated on silicon, without compromises on the performances of either the platforms.

1. Introduction

Silicon quantum photonics has garnered much attention in recent decades [1]. The optical transparency of silicon and the large refractive index contrast between silicon and silicon dioxide in the telecommunication wavelengths make silicon a good material to form submicron-scale waveguides, which subsequently paves the way for the implementation of photonic integrated circuits (PICs) with a high integration density. Moreover, the natural abundance and the mature CMOS process technology also enable large-scale, low-cost manufacturing of the PICs [2].

The main challenge in realizing silicon quantum photonics is that there is no native efficient on-demand single-photon source (SPS) available due to the indirect band-gap nature of silicon [3]. Currently, quantum light on silicon is either generated via probabilistic processes such as parametric down-conversion [4], or injected from off-chip sources interfaced with optical fibers [5]. Nonetheless, direct integration of III–V semiconductor quantum dots (QDs) based SPS, which offer outstanding optical emission properties such as high indistinguishability, single-photon purity, entanglement fidelity, and brightness, on a silicon platform, can provide interesting outlooks to increase the experimental complexity [6].

SPSs in the form of III–V QDs have already been transferred onto a range of integrated platforms, including systems based on silicon, silicon nitride, and lithium niobate, to name a few, by employing various techniques such as wafer bonding [7], transfer printing [8] and pick-and-place technology [9, 10]. Despite all

these approaches, monolithic integration, i.e. the direct growth of III–V materials on silicon, is the most desired approach because it is economically favorable and allows high-density integration. However, it is very challenging because of the large lattice mismatch, material polarity, and coefficient of thermal expansion (CTE) difference between the III–V materials and silicon [11, 12]. One way to accommodate the lattice and CTE mismatches, as well as to mitigate the defects, is to integrate a thick intermediate buffer layer between the III–V active region and silicon [13]. However, this requirement hinders the implementation of the low-loss evanescent light coupling scheme to effectively couple the light between III–V semiconductors and silicon-on-insulator waveguides.

An alternate monolithic approach for large-scale integration of III–V materials is through heterogeneous integration of thin III–V membrane using a direct bonding technique followed by epitaxial regrowth [14–19]. This integration scheme is promising because it can overcome the challenges of the conventional monolithic integration approach, such as the high-density threading dislocation and anti-phase domain. Furthermore, the thin bonded membrane also allows the implementation of the low-loss evanescent light coupling scheme. Moreover, it is also possible to perform multiple sequential regrowths on the same bonded template for the integration of various epitaxial structures for high-density integration [20].

In previous studies, we have developed a material system of InAs QDs on GaAs substrate with a non-linear metamorphic buffer (MMB) layer in between them. With this approach, the highly developed In(Ga)As QDs system was engineered to emit up to the telecom C-band [21–24]. In this work, we report on the integration of the telecom C-band emitting InAs QDs on a wafer-bonded GaAs/Si template using metal-organic vapor-phase epitaxy (MOVPE) as a starting point for establishing hybrid III–V/Si PICs. While previous works required the use of thick III–V templates for high-quality QDs growth, which rendered difficulties in achieving efficient evanescent coupling with underlying silicon photonics, here we demonstrate that single telecom QDs can be effectively grown on silicon using a thin III–V and MMB template. To the best of our knowledge, this is the first demonstration of the integration of self-assembled single InAs QDs onto a silicon platform using the epitaxial regrowth on the III–V-on-Si bonded template approach.

2. Fabrication of GaAs/Si template

For the fabrication of the GaAs/Si template, we used the commercially available prime quality, single-side polished 2-inch (100) n-GaAs and undoped-Si wafers. First, a 1 μm thick $Al_{0.7}GaAs$ etch stop layer followed by 100 nm of GaAs was grown on the GaAs wafer using MOVPE, as shown in figure 1 (stage I). The as-grown sample surface exhibited a root-mean-square (RMS) roughness, R_q of 0.18 nm from an atomic force microscopy (AFM) scan measured over a $20 \times 20\,\mu m^2$ area. This value is well below the general roughness limit of 0.5 nm, which has to be satisfied to achieve successful direct bonding on a wafer-scale [25, 26].

Prior to plasma activation in the oxygen plasma asher, the surfaces of the as-grown sample and the Si wafer were subjected to a cleaning process using organic solvents, acetone and isopropyl alcohol (IPA), to remove the organic contaminants on the surface in order to maximize the bonding yield. The surfaces were additionally treated with 1% hydrofluoric acid (HF) to remove the native oxides. Following the cleaning processes, the surfaces were exposed to oxygen plasma to form an ultra-thin oxide layer, to promote the smoothness and hydrophilicity of the surfaces before the bonding process. The surfaces were then brought into contact for the purpose of direct bonding, as illustrated in figure 1 (stage II).

Once the wafers were bonded, the wafer stack was annealed under a vacuum environment to replace the hydrogen bonds with stronger covalent bonds [27]. The annealing process began at room temperature and involved a gradual increase in temperature over a period of 6 h to reach 200 °C. After reaching 200 °C, the wafer stack was annealed at this temperature for a duration of 6 h. Following that, there was a slow ramping down over the course of 6 h to return to room temperature. The gradual increase and decrease in temperature during annealing was implemented to avoid debonding or cracking of the wafers.

To obtain the GaAs/Si template, the original GaAs substrate and the $Al_{0.7}GaAs$ etch stop layer were selectively removed by wet-chemical etching using citric acid with H_2O_2 in a 4:1 solution and 10% HF acid, respectively. The GaAs/Si template was cleaned using a mixture of potassium hydroxide (KOH) and deionized water, followed by rinsing in IPA to remove the etching residues on the surface [28]. Figures 2(a) and (b) depict the scanning electron microscope (SEM) scan of the GaAs/Si template before and after the cleaning process, respectively, where the RMS roughness of the surface from AFM scans significantly decreases from 4.74 nm to 0.49 nm.

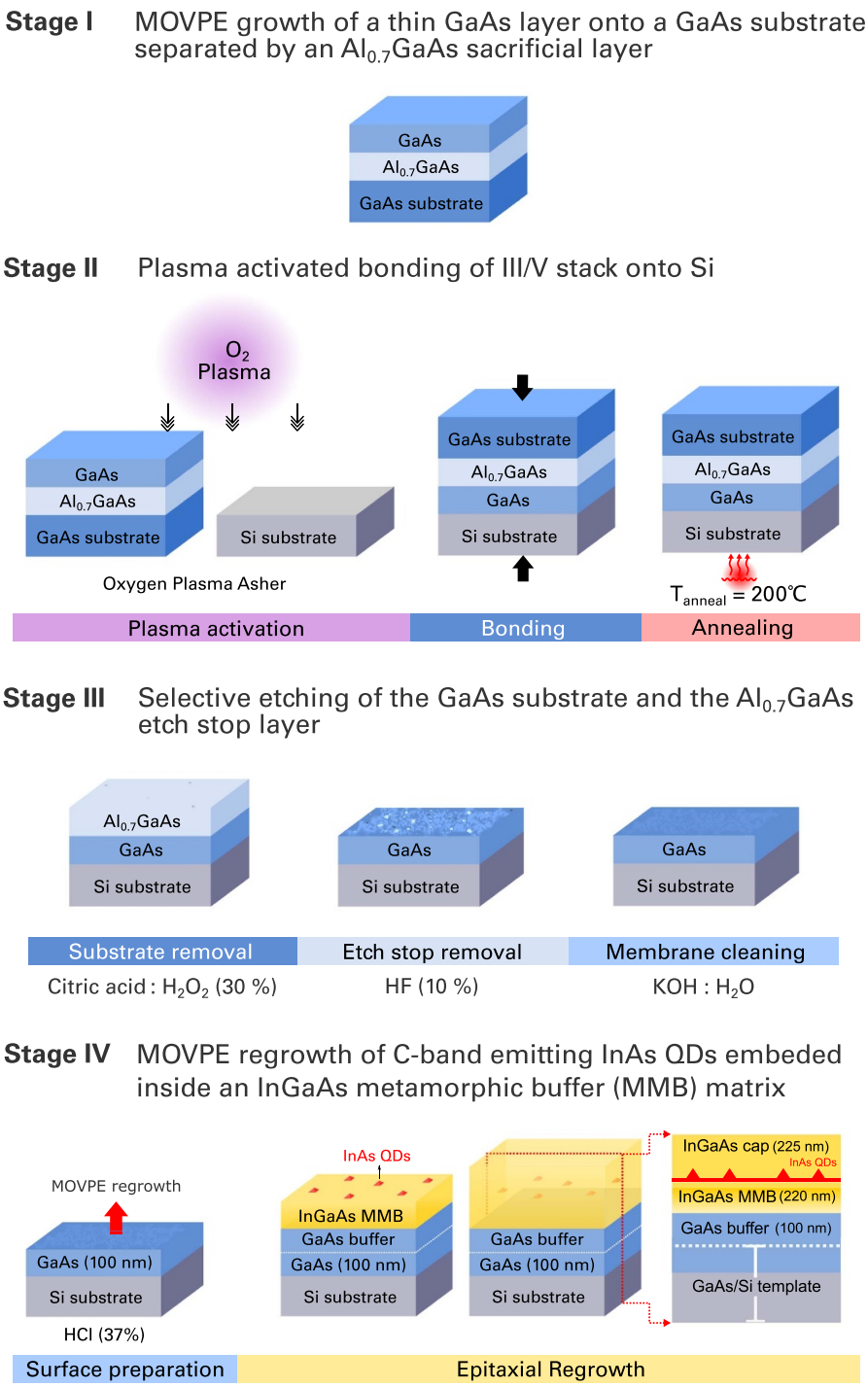

Figure 1. Schematic diagram depicting the process flow for the fabrication of GaAs/Si template (stages I–III) and the epitaxial regrowth of InAs QDs on the fabricated GaAs/Si template (stage IV).

3. Epitaxial regrowth on GaAs/Si template

We employed the fabricated GaAs/Si template to grow telecom C-band emitting InAs QDs. Prior to the process of epitaxial regrowth, the template was subjected to a 37% hydrochloric acid (HCl) treatment for a duration of 60 s to remove the native oxides present on the surface of the template. The treated template was promptly loaded into the MOVPE reactor to prevent any further re-oxidation of the surface. The epitaxial growth process was performed using a commercially available AIX-200 horizontal MOVPE system. The growth was carried out at a reactor pressure of 100 mbar, using the standard precursors trimethylgallium (TMGa), trimethylindium (TMIn), and arsine (AsH_3). Hydrogen gas (H_2) was used as the carrier gas. To limit the defects arising from the disparity in the CTE between GaAs and Si, the growth temperature was

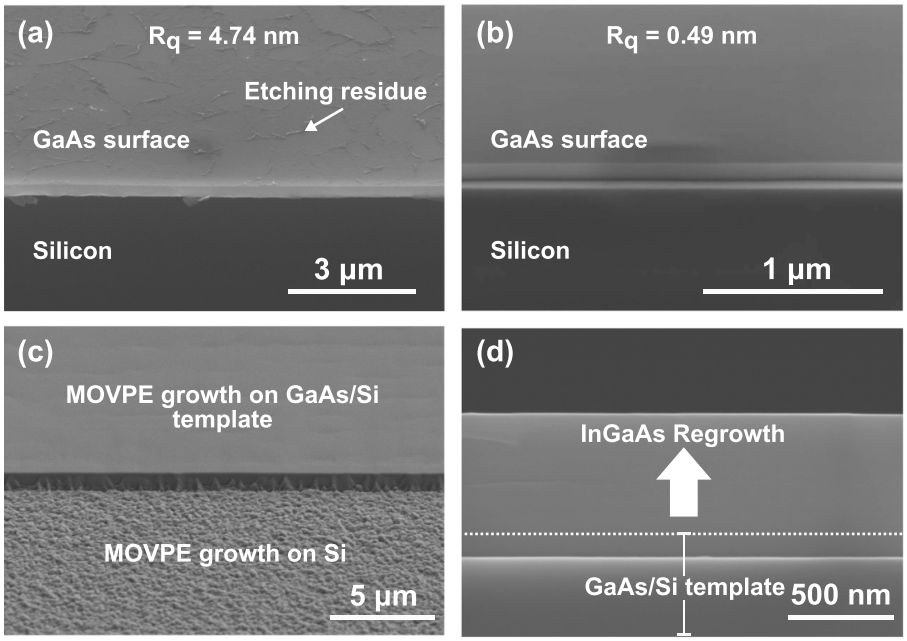

Figure 2. SEM scans of the perspective view of the GaAs/Si template (a) before and (b) after the cleaning process. SEM scans of the (c) perspective and (d) cross-sectional view of epitaxial structure grown on GaAs/Si template.

ensured not to exceed 595 °C at any point during the epitaxy (following a similar argument as in [29]). Furthermore, in order to prevent the cracking and buckling of the bonded GaAs membrane, a gradual heating (0.95 °C s^{-1}) and cooling (0.6 °C s^{-1}) procedure was implemented at the start and the end of the epitaxy, respectively.

The growth structure consists of a GaAs buffer layer with a thickness of 100 nm (which can be reduced or even fully removed if necessary), followed by a thin InGaAs MMB layer with a thickness of 220 nm [22], InAs QDs, and an InGaAs cap layer with a thickness of 225 nm. The schematic of the epitaxial layer structure grown on the GaAs/Si template is depicted in figure 1 (stage IV).

4. Results

4.1. Surface characterization

Figures 2(c) and (d) show the perspective and cross-sectional SEM scans of the epitaxial structure grown on the GaAs/Si template, respectively. A high-quality crystal growth on the part where the thin GaAs membrane was present and a continuous polycrystalline epitaxial growth on the part where the GaAs membrane was intentionally removed can be seen (figure 2(c)). The polycrystalline growth in the latter case is due to the suboptimal nucleation and bulk growth conditions for the direct growth on silicon.

Furthermore, AFM characterization was also employed to conduct a comparative study on the surface quality of the epitaxial structure grown on the GaAs/Si template and on a standard GaAs substrate, which served as a reference. The surface morphology of the grown epitaxial structure was similar and comparable to one another with a cross-hatch pattern, characteristic of MMB structures, dominating the entire surface. The surface of the structure grown on GaAs/Si template exhibited a slightly lower RMS roughness, see figure 3, which will be explained in section 4.2. This verifies that with this integration approach, a high crystal quality growth of III–V semiconductor on silicon can be achieved, comparable to the well-established growth on GaAs, without the need for a thick intermediate buffer layer.

4.2. Optical characterization

The emission characteristics of the QDs were investigated in a standard low-temperature (4 K) ensemble-photoluminescence (PL) setup. Figure 4 compares the PL spectra of the InAs QDs grown on the GaAs/Si template and on a standard GaAs substrate under non-resonant excitation.

The peak PL intensity of the QDs grown on the GaAs/Si template was 1.2 times larger than that of the reference. The slight enhancement in the PL emission can be attributed to a small QD density change

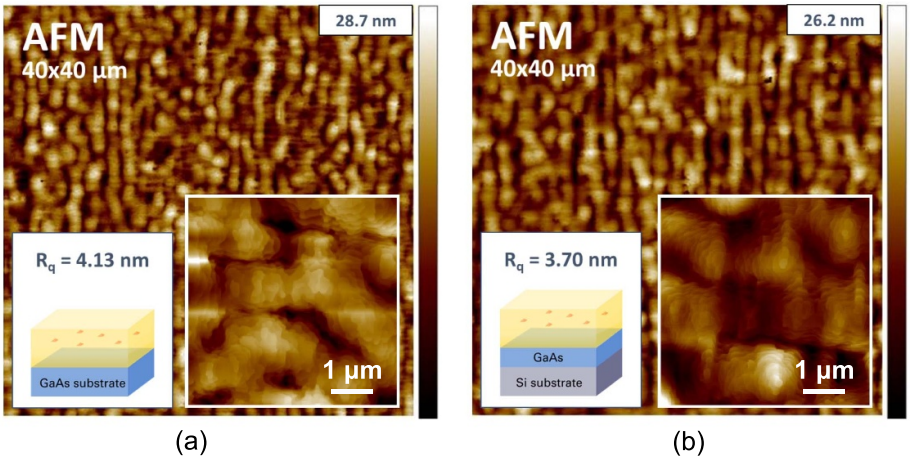

Figure 3. AFM scan of the epitaxial structure grown on (a) the standard GaAs substrate and (b) the fabricated GaAs/Si template.

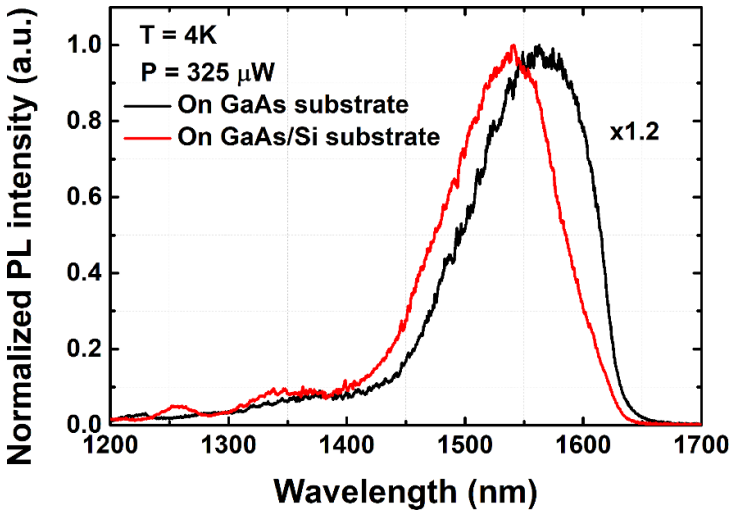

Figure 4. Normalized ensemble PL spectra of the InAs QDs grown on the GaAs/Si template and on a standard GaAs substrate. The ensemble grown on Si is 1.2 times larger than the reference structure.

between the samples. Nevertheless, in both cases, single QD emission can be observed (see the following). Although the profile of the PL spectra is similar, a shift in the PL peak toward a lower wavelength was observed for the QDs grown on the GaAs/Si template. The observed blueshift in the PL emission wavelength can be attributed to diminished indium incorporation during the MMB layer growth, due to the compressive strain present in the system arising from the mismatch in the CTE between GaAs and Si. This is also evident from the AFM characterization, where the surface roughness of the structure grown on GaAs/Si template is slightly lower than the reference structure, corresponding to an InGaAs semiconductor matrix with lower indium content. Additionally, to verify this, the telecom C-band emitting InAs QDs were also grown on GaAs/Si template and standard GaAs substrate simultaneously, on the same epitaxial run, and a recurrence of the above-mentioned trend in the PL emission spectra was observed. Furthermore, this wavelength shift can also arise from different growth conditions on a substrate with different strain which can also influence the stoichiometry and size of the QDs.

Additionally, micro-PL (μ-PL) measurements were performed at 6 K under a non-resonant excitation to characterize further the QDs grown on the GaAs/Si template and on a standard GaAs substrate. Figure 5 displays the collection of exemplary μ-PL spectra obtained from the samples mentioned above. In both cases, the μ-PL spectra exhibit sharp and distinct emission peaks, which correspond to the single QD lines, across the entire spectrum within the telecom C-band. The QDs from both samples have similar count rate and comparably narrow linewidth on the spectrometer, which implies that the quality of the QDs is similar in both cases.

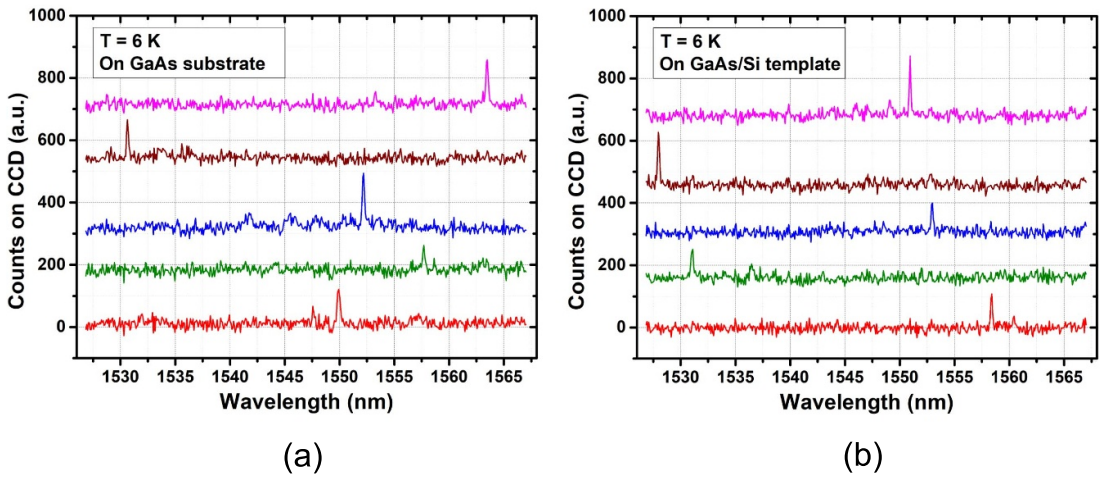

Figure 5. μ-PL spectra showing emission of single QDs at the telecom C-band for the InAs QDs grown on (a) a standard GaAs substrate and (b) the fabricated GaAs/Si template. The spectra are vertically shifted for clarity.

5. Conclusion

In this work, we have successfully integrated a thin GaAs membrane onto Si using a direct bonding method to fabricate a GaAs/Si template. The fabricated template was used for the epitaxial regrowth of InAs QDs emitting in the telecom C-band. The surface characterization measurements revealed that the quality of the crystal grown on GaAs/Si is comparable to the growth on a standard GaAs substrate, in terms of their surface roughness. Additionally, the optical characterization demonstrated that the InAs QDs grown on GaAs/Si are comparable to those grown on a standard GaAs substrate, in terms of their intensity and spectrometer linewidth. In conclusion, this integration method is a very promising approach for establishing hybrid III–V/Si quantum PICs, because it overcomes the problems of the conventional monolithic integration method. Furthermore, thanks to the thin intermediate layer between the QDs and the silicon substrate, it will be possible to fabricate single InGaAs waveguides directly on the silicon chip, enabling the development of high-complexity III–V/Si quantum PICs.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

Acknowledgments

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Conflict of interest

The authors declare no conflict of interest.

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